CLAIMS

What is claimed is:

1. An integrated circuit comprising

a first counter clocked by a clock signal having a nominal first period and provided by an oscillator external to the circuit;

a second counter clocked at a second period by an oscillator internal to the circuit, the second counter being reset each time the content of the first counter reaches a first predetermined value; and

means for activating an alert signal when the second counter reaches a second predetermined value such that the product of the second predetermined value by the second period is greater than the product of the first predetermined value by the first period.

2. The integrated circuit of claim 1 wherein the alert signal is activated when an actual period of the clock signal is greater than a threshold period, the product of the second predetermined value by the second period being smaller than the product of the first predetermined value by the threshold period.

3. The integrated circuit of claim 2 wherein the second period ranges between a lower limit and an upper limit, the product of the second predetermined value by the lower limit being greater than the product of the first predetermined value by the first period and the product of the second predetermined value by the upper limit being smaller than the product of the first predetermined value by the threshold period.

4. The circuit of claim 1 wherein the internal oscillator is formed of an odd number of series-connected inverters including a last inverter having an output connected to an input of a first one of the inverters.

5. The circuit of claim 1, further comprising a comparator that resets the second counter by generating a reset signal each time the content of the first counter reaches the first predetermined value.

6. The circuit of claim 5 wherein the first predetermined value is 2^n, and wherein the comparator comprises:

an AND gate having a first input that receives a bit of rank n of the first counter, an inverting second input, and an output that generates the reset signal; and

a D flip-flop clocked by the external oscillator and receiving said bit of rank n as an input, the D flip-flop having an output connected to the second input of the AND gate.

7. The circuit of claim 1, further comprising a functional block that enables implementation of a predetermined function until the content of the first counter reaches a predetermined limit, or until the alert signal is activated.

8. A method of time measurement using a counter provided to be clocked at a nominal first period by an oscillator, comprising the steps of:

clocking a second counter at a second period, the second counter being provided to be reset each time the content of the first counter reaches a first predetermined value; and

activating an alert signal when the second counter reaches a second predetermined value such that the product of the second predetermined value by the second period is greater than the product of the first predetermined value by the first period.

9. The method of claim 8 wherein the alert signal is activated when an actual period of the clock signal is greater than a threshold period, the product of the

second predetermined value by the second period being smaller than the product of the first predetermined value by the threshold period.

10. The method of claim 9 wherein the second period ranges between a lower limit and an upper limit, the product of the second predetermined value by the lower limit being greater than the product of the first predetermined value by the first period and the product of the second predetermined value by the upper limit being smaller than the product of the first predetermined value by the threshold period.

11. The method of claim 8 wherein resetting the second counter includes:

clocking a D flip-flop using the oscillator;

receiving a bit of rank n of the first counter at an input of the D flip-flop;

receiving the bit of rank n at a first input of an AND gate;

receiving an output of the D flip-flop at an inverting second input of the AND gate; and

providing a reset signal from an output of the AND gate to the second counter in response to the bit of rank n switching logic states.

12. The method of claim 8, further comprising ending implementation of a predetermined function in response to the content of the first counter reaching a predetermined limit, or the alert signal being activated.

13. A method for managing a time-limited right of implementation of a predetermined function, the method comprising:

time using a counter provided to be clocked at a nominal first period by a quartz oscillator;

clocking a second counter at a second period, the second counter being provided to be reset each time the content of the first counter reaches a first predetermined value;

activating an alert signal when the second counter reaches a second predetermined value such that the product of the second predetermined value by the second period is greater than the product of the first predetermined value by the first period; and

causing the implementation of the predetermined function to end in response to the content of the first counter reaching a predetermined limit, or the alert signal being activated.

14. An integrated circuit for determining that a first clock signal, output by an external oscillator, has obtained an threshold first period that is greater than a nominal first period of the external oscillator, the integrated circuit comprising:

a first counter having a clock output and a clock input that receives the first clock signal;

an internal oscillator having an output that provides a second clock signal having a second period;

a second counter having a clock input coupled to the output of the internal oscillator, a reset input coupled to the first counter; and an output, the second counter being reset each time the output of the first counter reaches a first predetermined value; and

a comparator having an input coupled to the output of the second counter and an output that activates an alert signal when the second counter reaches a second predetermined value, the second predetermined value being greater than the first predetermined value multiplied by the nominal first period and divided by the second period.

15. The integrated circuit of claim 14 wherein the second period ranges between a lower limit and an upper limit, the second predetermined value being greater than the first predetermined value multiplied by the nominal first period divided by the lower limit, and the second predetermined value being smaller than the first predetermined value multiplied by the threshold first period divided by the upper limit.

16. The integrated circuit of claim 14 wherein the internal oscillator is formed of an odd number of series-connected inverters including a last inverter having an output connected to an input of a first one of the inverters.

17. The integrated circuit of claim 14, further comprising an additional comparator connected between the output of the first counter and the reset input of the second counter, the additional comparator being structure to reset the second counter by generating a reset signal each time the output of the first counter reaches the first predetermined value.

18. The integrated circuit of claim 17 wherein the first predetermined value is 2^n, and wherein the additional comparator comprises:

an AND gate having a first input that receives a bit of rank n of the first counter, an inverting second input, and an output that generates the reset signal; and

a D flip-flop clocked by the external oscillator and receiving said bit of rank n as an input, the D flip-flop having an output connected to the second input of the AND gate.

19. The circuit of claim 14, further comprising a functional block coupled to the first counter and the comparator and structured to end implementation of a predetermined function in response to the output of the first counter reaching a predetermined limit, or the alert signal being activated.